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(54) Process of cleaning silicon prior to formation of the gate oxide

(57) The process involves an improved pre-gate cleaning technique that results in a smoother wafer surface than previous techniques. In particular, the pre-gate cleaning technique involves a step of rinsing a silicon wafer with ozonated water. Typically, the technique

involves the sequential steps of cleaning the silicon wafer with HF, performing the ozonated water rinse, and treating with an SC1 solution. The oxygen in the ozonated water induces formation of a more uniform chemical (as opposed to native) oxide layer, which etches more uniformly in the SC1

FIG. 2



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Description

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The invention relates to a process for semiconductor device fabrication, in particular, steps involving cleaning of a silicon substrate prior to formation of a gate oxide.

Discussion of the Related Art

[0002] One step involved in semiconductor device fabrication is cleaning of silicon wafer substrates before further processing steps, e.g., before formation of a gate oxide. Such cleaning is performed to remove particulate contaminants, organics, and/or metals as well as any native oxide, both of which tend to interfere with subsequent processing. In particular, insufficient cleaning is detrimental to the properties of the gate oxide, which in turn affect the properties of the entire device.

[0003] Various procedures are used to clean silicon wafers. A widely-used procedure is the standard RCA clean. The RCA clean involves exposure to three separate solutions - SC1, HF, and SC2. An SC1 solution contains ammonium hydroxide, hydrogen peroxide, and water, and is generally effective at removing particles and metals from a silicon wafer surface. An SC2 solution contains hydrochloric acid, hydrogen peroxide, and water, and is generally effective at removing alkali ions as well as metal hydroxides that are insoluble in ammonium hydroxide. The HF strips any native oxide from the surface.

[0004] Many varieties of the RCA clean exist, but are still referred to as an RCA clean due to use of the SC1 and/or SC2 solution. A typical RCA clean involves the sequential steps of: HF → a deionized water rinse → SC1 → a deionized water rinse → SC2 → a deionized water rinse. It is also possible to perform the steps in different order, e.g., reversing the order of the HF and SC 1 steps, or to omit a step, e.g., omit the SC2 step.

[0005] A problem with RCA cleans, however, is that SC1 solutions have a tendency to cause roughening of the silicon surface, due to the presence of OH⁻ in the SC1 solution. (See Higashi and Chabal, "Silicon Surface Chemical Composition and Morphology," Handbook of Semiconductor Wafer Cleaning Technology, Noyes Publications (1993).) And it is possible for such roughening to interfere with device performance, particularly as device sizes and spacings become smaller.

[0006] Pre-gate cleans that do not roughen the silicon surface are therefore desirable.

SUMMARY OF THE INVENTION

[0007] The invention provides a process involving an improved cleaning technique that results in a smoother

surface than previous techniques. In particular, the cleaning technique of the invention involves a step of rinsing a silicon wafer with ozonated water. (Ozonated water typically comprises 5 to 20 ppm ozone dissolved in deionized water.) Typically, the cleaning technique involves the sequential steps of cleaning the silicon wafer with HF, performing the ozonated water rinse, and treating with an SC1 solution. It is possible to omit the initial HF cleaning step.

[0008] It is believed that the advantageous smoothness is attained as follows. Where an HF rinse is performed, the HF strips any native oxide from the silicon surface. The ozone induces formation of a more uniform chemical (as opposed to native) oxide layer, and this chemical oxide thus etches more uniformly in the SC1 than a native oxide. The resulting silicon thereby exhibits a surface smoothness higher than would be attained in an equivalent process without the ozonated water step. Where the HF rinse is omitted, the ozonated water similarly induces formation of an oxide layer that results in a more uniform etch by the SC1.

[0009] Subsequent device processing steps are thus able to be performed on a smoother surface than obtained by previous cleaning techniques, thereby contributing to improvement in the overall device.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] Fig. 1 shows the initial surface of a silicon wafer.

[0011] Fig. 2 shows the surface of a silicon wafer after treatment according to the invention.

[0012] Fig. 3 shows the surface of a silicon wafer after a conventional treatment.

DETAILED DESCRIPTION OF THE INVENTION

[0013] In one embodiment of the invention, a silicon wafer is treated as follows. First, the wafer is treated to an HF rinse. The concentration of HF is typically 0.5 to 10% HF in water. The HF is effective in removing any native oxide that may be present on the wafer. Such oxides (whether native or chemical) are normally present in commercially-obtained wafers. (Specifically, a wafer manufacturer generally leaves a native oxide in place or provides a chemical oxide to protect the silicon surface.) The HF rinse is performed by any suitable technique, e.g., dipping or spraying. (As noted above, it is possible to omit the HF rinse.)

[0014] Second, the wafer is treated - typically rinsed - with ozonated, deionized water. The dissolved O₃ in the ozonated water induces formation of a relatively uniform chemical oxide layer on the wafer. The oxide layer is generally about 8Å to about 12Å thick, and generally has a surface roughness that is substantially unchanged from that of the starting substrate. The ozonated water rinse is performed by any standard technique, including cycles of quick dump and/or overflow rinse. The partic-

ular technique, however, does not appear to impact the increased smoothness attained by the process of the invention.

[0015] Third, the wafer is treated with an SC1 solution. Typically the SC1 solution has a concentration ratio of 1:1:5 to 1:10:100 ($\text{NH}_4\text{OH}:\text{H}_2\text{O}_2:\text{H}_2\text{O}$), although it is possible to widely vary these relative concentrations and still attain a desired result. Control runs are easily performed to determine an appropriate ratio for a given set of process parameters. The SC1 removes particles, organics, and metals from the wafer surface, and is performed by any suitable technique.

[0016] Typically, an SC1 treatment would introduce some roughness into a wafer surface. But the presence of the chemical oxide layer induced by the ozonated water appears to keep the SC1 etch relatively uniform. Specifically, the native oxide found on a silicon wafer is less uniform than a chemically-formed oxide layer. Thus, it is believed the SC1 affects the native oxide in a non-uniform manner, resulting in increased surface roughness. In the invention, however, the presence of the more uniform chemical oxide layer tends to cause the SC1 etch to take place in a more uniform manner. (This is true even if the initial oxide is not removed by an HF rinse.) The process generally provides a silicon wafer with a surface roughness substantially unchanged from (typically identical to) that of the starting substrate.

[0017] The SC1 treatment is followed by a deionized water rinse. The wafer is then ready for gate oxide formation, and subsequent device formation steps, as is known in the art. (See, e.g., S.M. Sze, VLSI Technologies, McGraw-Hill (1988).)

[0018] Optionally, other pre-gate cleaning steps are performed, e.g., SC2 rinse. It is possible to use additional or alternative chemistries as well. For example, chemistries that provide the same result as the SC1 rinse, i. e., removal of particles, organics, and metals, are possible. Alkaline cleaning solutions, typically with a pH above 8.5, are typically suitable, e.g., tetramethylammonium hydroxide.

[0019] Thus, the ozonated water treatment is useful with a variety of techniques used for pre-gate cleans.

[0020] The invention will be further clarified by the following examples, which are intended to be exemplary.

Example 1

[0021] A silicon wafer with native oxide, having a surface roughness of 0.6 Å rms was obtained (as measured by atomic force microscopy - AFM). An AFM image of a 0.6 Å rms silicon wafer is shown in Fig. 1. (All AFM images in the examples cover an area of 2 µm x 2 µm and a height range of 1 nm.) The following process was performed:

(a) HF rinse (15:1 water to HF) at room temperature for 30 seconds;

(b) deionized ozonated water rinse (10 ppm ozone) for 10 minutes at room temperature, using an overflow rinse;

(c) SC1 rinse at a concentration ratio of 1:8:64 ($\text{NH}_4\text{OH}:\text{H}_2\text{O}_2:\text{H}_2\text{O}$) for 10 minutes at 65°C using a technique of SC1 immersion with megasonic energy; and

(d) deionized water rinse at room temperature for 10 minutes, using 6 cycles of overflow/quickdump rinse technique.

[0022] The resulting surface exhibited a surface roughness of 0.6 Å rms - the same as the initial surface, as shown in the AFM image of Fig. 2.

Comparative Example 2

[0023] Using a silicon wafer having a surface roughness of 0.6 Å rms, such as shown in Fig. 1, the following process was performed:

(a) SC1 rinse at a concentration ratio of 1:8:64 ($\text{NH}_4\text{OH}:\text{H}_2\text{O}_2:\text{H}_2\text{O}$) for 10 minutes at 65°C using a technique of SC1 immersion with megasonic energy; and

(b) deionized water rinse at room temperature for 10 minutes, using 6 cycles of overflow/quickdump rinse technique;

(c) HF rinse (15:1 water to HF) at room temperature for 30 seconds;

(d) deionized water rinse at room temperature for 10 minutes, using 6 cycles of overflow/quickdump rinse technique.

[0024] The resulting wafer exhibited a surface roughness of 1.0 Å rms, substantially higher than the initial roughness, as shown in the AFM image of Fig. 3.

[0025] Other embodiments of the invention will be apparent to those skilled in the art from consideration of the specification and practice of the invention disclosed herein.

Claims

1. A process for fabricating an article, comprising the steps of: providing a silicon wafer;

treating the wafer with ozonated water, such that an oxide forms on the wafer surface; and performing an etch of the treated wafer to substantially remove from the wafer surface at least one impurity selected from particles, organic materials, and metals.

2. The process of claim 1, wherein the ozonated water comprises deionized water and 5 to 20 ppm ozone.

3. The process of claim 1, wherein the etch is performed with an SC1 solution.
4. The process of claim 1, wherein an HF rinse of the wafer is performed prior to the ozonated water treatment. 5
5. The process of claim 1, wherein the process is performed in the absence of an HF rinse of the wafer. 10
6. The process of claim 1, wherein the surface roughness of the wafer after the etch is performed is the same as the roughness of the wafer prior to the treatment with the ozonated water. 15

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FIG. 1

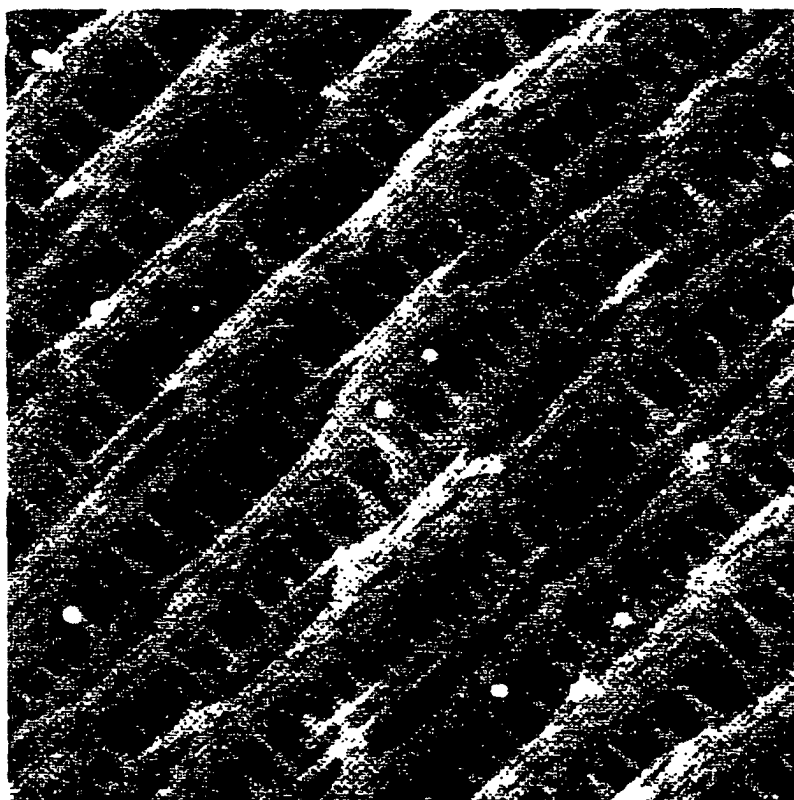


FIG. 2

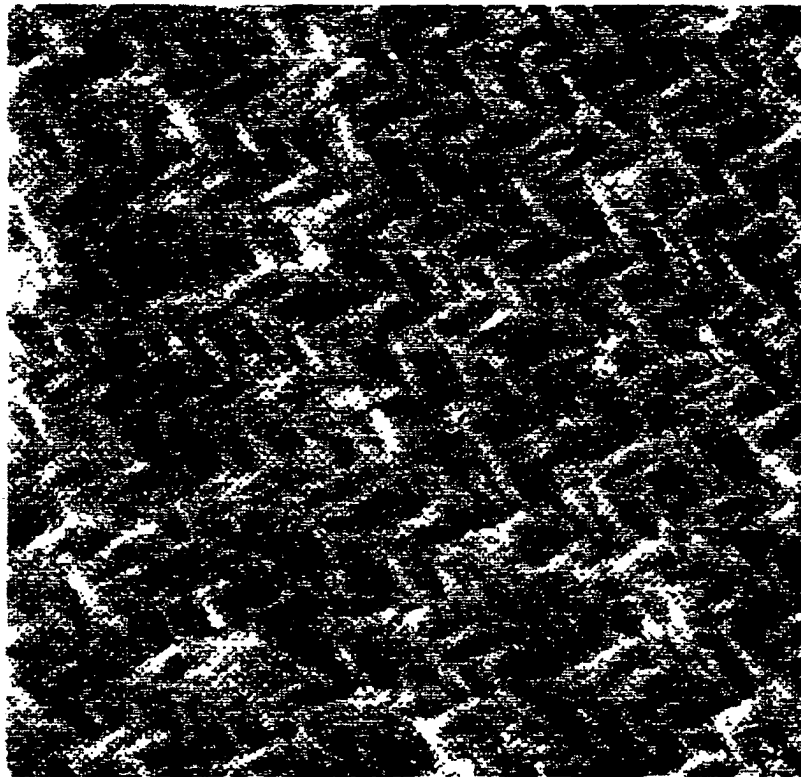
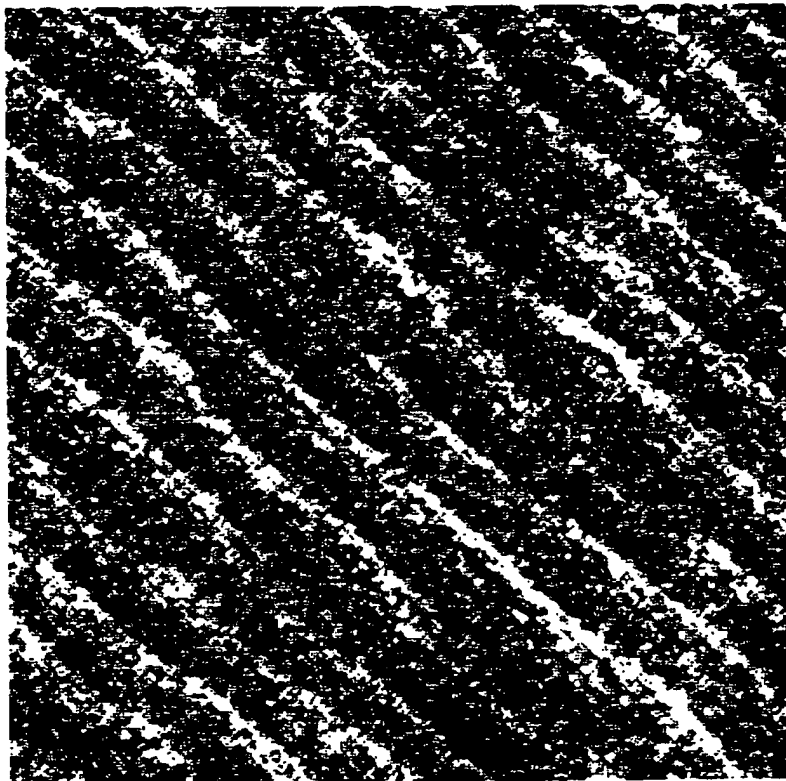


FIG. 3





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EUROPEAN SEARCH REPORT

Application Number
EP 00 30 8689

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| The present search report has been drawn up for all claims | | | |
| Place of search THE HAGUE | | Date of completion of the search 5 June 2001 | Examiner Gorl, P |
| CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document | | | |

EPO FORM 1503 (3.9.97) (P04/01)



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EUROPEAN SEARCH REPORT

Application Number
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| <p>CATEGORY OF CITED DOCUMENTS</p> <p>X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document</p> <p>T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document</p> | | | |

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**ANNEX TO THE EUROPEAN SEARCH REPORT
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05-06-2001

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For more details about this annex : see Official Journal of the European Patent Office, No. 12/82